Ind.D.K376SBC.00 Rev. 2.0

High Performance 68376 CPU board

General description

The K376SBC is a general purpose, low cost single board system built around the MC68376 microcontroller running at 22 MHz (figure 1). In addition to the MC68376, the K376SBC includes 1 MBytes of static RAM, 1 MBytes of Flash (640 KByte for the KOS and 384 KBytes for user data or applications). A serial 9 pin DCE RS232 interface is used as a primary communication channel with the board. Different serial and parallel extensions (SXB Serial eXtension Bus, CXB CPU eXtension Bus and IXB Interface eXtension Bus) are also available and commented in detail in this document. The combination of high functionality and low power consumption makes the board ideally suited for applications in embedded and automotive control and in portable instrumentation.

Features

- MC68376 20 MHz microcontroller.
- 1 MBytes of CMOS static RAM.
- 1 MBytes of Flash.
- Fast MMA interface (Multi-Microcontroller Adapter) for multi CPU applications.
- DC/DC converter on board.
- 16 10 bit resolution analog inputs.
- 16 TPU I/Os.
- Serial eXtension Bus (SXB).
- 9 pin DCE RS232 interface.
- K-Net local network.
- CPU eXtension Bus (CXB).
- Interface eXtension Bus (IXB).
- Wide power supply input (DC/DC) +8.5 V to +20 V less than 1 W typ. at full speed (22 MHz).
- Size 128 x 89.9 mm.
- On board Multitasking Kernel KOS. Reference software K376KOS.

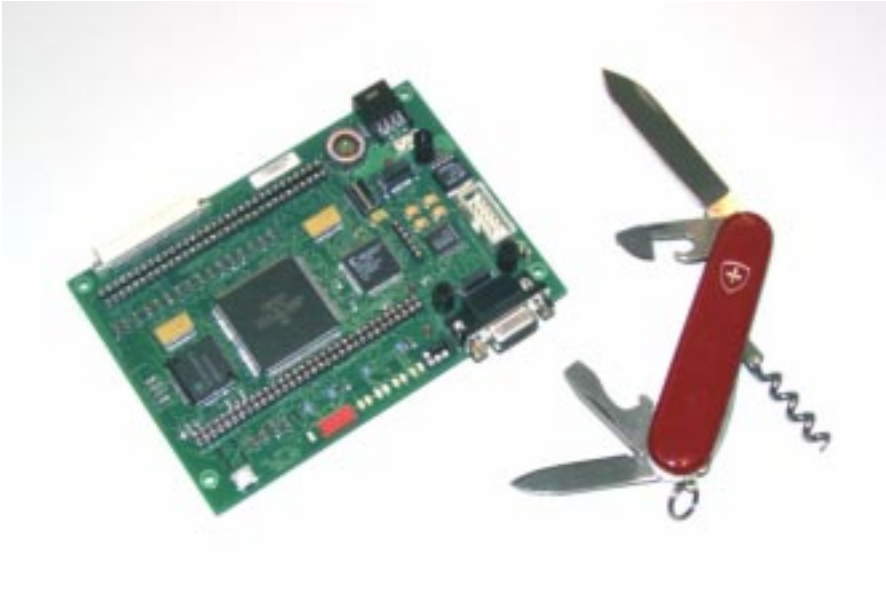

Figure 1: The K376SBC board

The bloc diagram

Figure 2 shows the block diagram of the board interfaces.

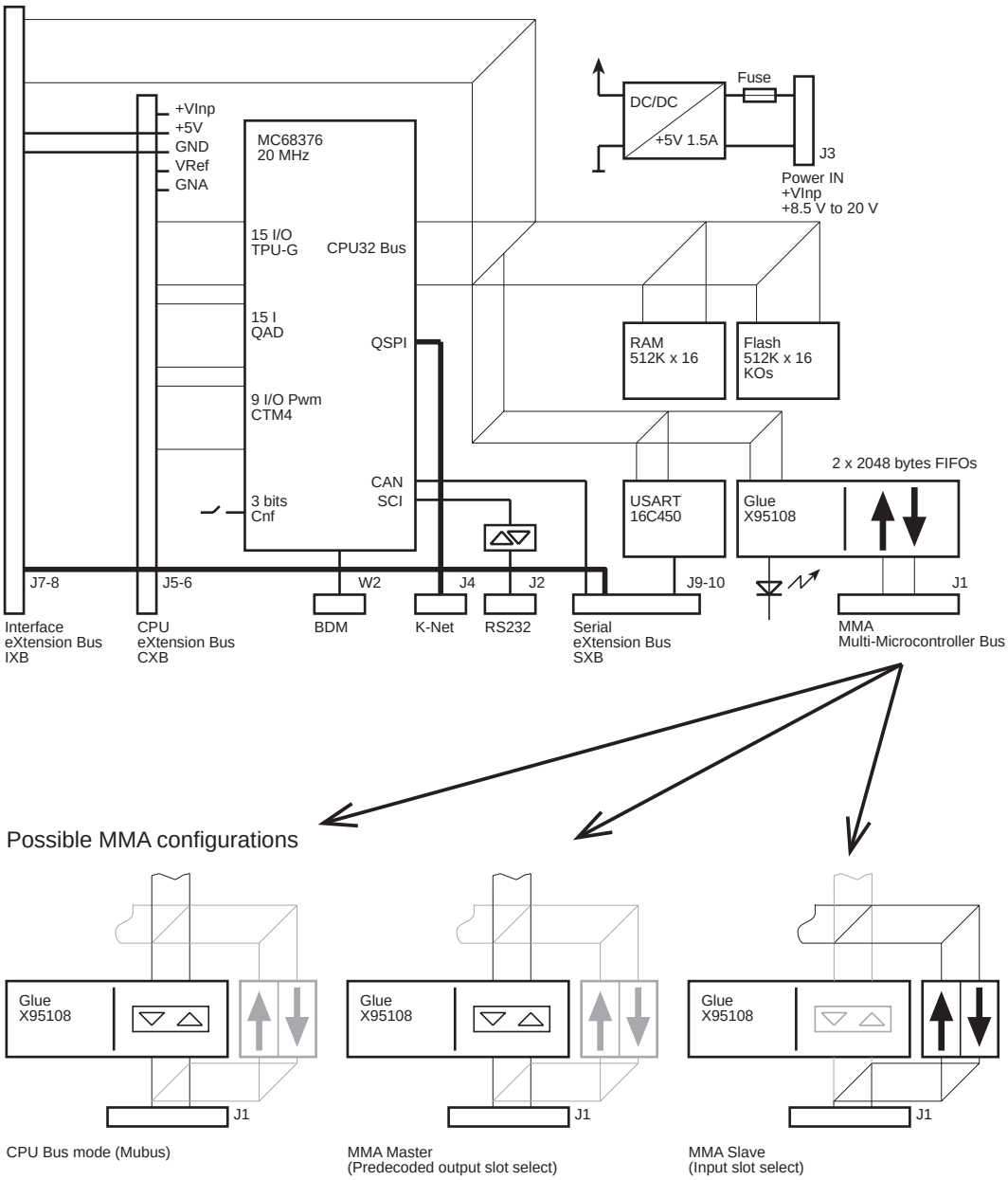

Figure 2: Block diagram of the K376SBC

Description of the board resources

The power supply

The power supply is realised with a DC-DC step-down converter. This allows to convert large input voltages (from +8.5 V to +20 V) to the main +5 V necessary to the board. In this range the efficiency can achieve 90% (see table 1 for the pinning connector).

J3: Input power supply connector			
AMP 2x4 pin male connector			
Signal	Pin	I/O	Comment
GND	1-2	Power	Digital ground.
VCC	3-4	Power	+5 V. This is an output voltage useable to power interfaces.
+VInp	5-6	Power	+8.5 V to +20 V
GNP	7-8	Power	Power ground. Digital and Power ground are connected inside the board.

Table 1: Power supply connector

The microcontroller

All the board functionalities are built around the MC68376 microcontroller. The internal clock of 20.9 MHz is generated by an external 4.192 MHz crystal coupled to the internal PLL. By software it is possible to slow-down the frequency to reduce the power consumption.

This microcontroller includes an impressive amount of modules making possible complex control applications in few cm^2. Here is the list of the included modules:

- CPU32: 68020 like CPU unit without cache.
- System Integration Module (SIM): it consists in five submodules that control the microcontroller start-up, initialisation, configuration and external bus with a minimum of external devices (system configuration and protection, clock synthesizer, chip-selects, external bus interface and system tests).
- Queued Serial Module (QSM): it provides the microcontroller with two serial communication interfaces divided into two submodules: the queued serial peripheral interface (QSPI) and the serial communication interface (SCI).
- Time Processor Unit (TPU): it is a semi-autonomous module designed for complex timing control. Operating simultaneously with the CPU, the TPU executes microinstructions (microcode) from TPU control ROM. Functions are microcode programs that typically schedule task and perform input and output operations. The TPU included inside the mounted chip has the version G.
- 4 KBytes of high speed CMOS RAM. When coupled with the TPU module this memory can contain an additional set of functions for the TPU. In a normal operation this memory can be used to execute downloaded routines in a very fast mode (fast termination mode).
- Configurable Timer Module (CTM4): it is a module containing timers, PWM generators, I/O for input capture and output compare functions.
- Queued Analog Digital Module (QADM): it is a semi-autonomous 16 inputs of 10 bits analog to digital converter.
- Background Debug Mode (BDM): microcontroller system generally provides a debugger, implemented in software for system analysis at the lowest level. The BDM on the CPU32 is unique because the debugger has been implemented in CPU microcode. To use BDM features it is necessary to connect the board to a host computer equipped with a dedicated hardware and software.
- Controller Area Network (CAN): it is a serial communication protocol that efficiently supports distributed real-time control with a very high level of data integrity.

The BDM Background Debug mode

The BDM is an interface for debugging. CPU registers as well as memory locations can be read or written. An out-board interface connected to a host (figure 3) is necessary to operate with it (see table 2 for the pinning connector).

J11: BDM connector			
3M 10 pin male connector			
Signal	Pin	I/O	Comment
/DS	1	Digital O	Data strobe.
/BErr	2	Digital O	Bus error.
GNP	3-5	Power	Digital ground.
/BKPT	4	Digital I	Signals an hardware break-point to the CPU.
/FREEZE	6	Digital O	Indicates that the CPU has acknowledged a breakpoint.
/Reset	7	Digital O/I	System reset.
/IFETCH	8	Digital O	Indicates when the CPU is performing an instruction word prefetch and when the instruction pipeline has been flushed.
VCC	9	Power	+ 5V.
/IPIPE	10	Digital O	Used to track movement of words through the instruc-tion pipeline.

Table 2: BDM connector

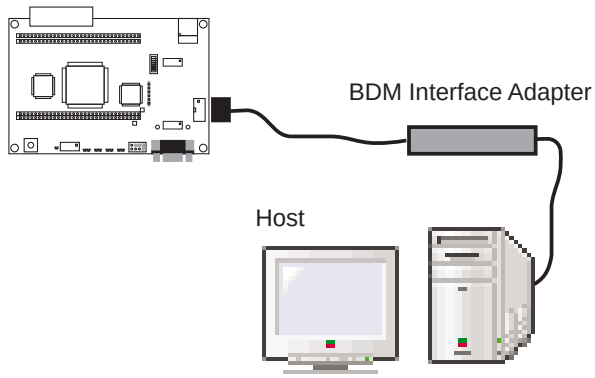

Figure 3: BDM connection

The primary RS232 channel

The main connection with the K376SBC is realised with a simplified DCE RS232 interface using the internal SCI module of the microcontroller. This channel does not support any hardware handshake capabilities (see table 3 for the pinning connector).

J2: Serial RS232 DCE connector			
Canon 9 pin female connector			
Signal	Pin	I/O	Comment
DCD	1	Digital O	Data Carrier Detect. Always fixed to high voltage.
RxD	2	Digital I	Receive data.
TxD	3	Digital O	Transmit data.
N.C	4-7		
GND	5	Power	Digital ground.
DSR	6	Digital O	Data Set Ready. Always fixed to high voltage.
CTS	8	Digital O	Clear To Send. Always fixed to high voltage.

Table 3: DCE RS232 connector

The Multi-Microcontroller Bus (MMA)

The Multi-Microcontroller Bus (MMA) is a fast interface designed to support asynchronous multi-processor applications. Each CPU board connected on this bus communicates or shares data via a couple of high speed fifos (see table 4 for the pinning connector).

J1: MMA connector (part of the connector)			
Erni 50 pin male connector			
Signal MMA mubus	Pin	I/O master/mubus slave	Comment
GND	B1	Power	Digital ground.
D0	A1	Digital I/O	CPU data 0.
D1	B2	Digital I/O	CPU data 1.
D2	A2	Digital I/O	CPU data 2.
D3	B3	Digital I/O	CPU data 3.
D4	A3	Digital I/O	CPU data 4.
D5	B4	Digital I/O	CPU data 5.
D6	A4	Digital I/O	CPU data 6.
D7	B5	Digital I/O	CPU data 7.
/Pm	A5	Digital O	Select Mubus.
+5 VPm	B6	Power	+5 V for Mubus (W4-8).
/INT	A6	Digital Im/Os	Interruption Req.
/W	B7	Digital Is/Om	CPU R/W.
/SLOT0M-A0m	A7	Digital Is/Om	Select slot 0 or CPU A0.
/SLOT1M-A1m	B8	Digital Is/Om	Select slot 1 or CPU A1.
A2	A8	Digital Is/Om	CPU address 2.
A3	B9	Digital Is/Om	CPU address 3.
/SLOT2M-A4m	A9	Digital Is/Om	Select slot 2 or CPU A4.
/SLOT3M-A5m	B10	Digital Is/Om	Select slot 3 or CPU A5.
N.C.	A10		
+12 V	B11	Power	+VInp. +8.5 V to +20 V.
GNP	A11	Power	Power ground.
+12 V	B12	Power	+VInp. +8.5 V to +20 V.
GNP	A12	Power	Power ground.
+12 V	B13	Power	+VInp. +8.5 V to +20 V.
GNP	A13	Power	Power ground.

Table 4: MMA/Mubus connector

This multi-processor scheme operates in a star configuration where the main (master) CPU is located in the center.

CPU independent architecture allows the connection of high speed units such a DSP, making possible performant applications.

According with the settings of W4-4..W4-7 this interface can be configured as described in table 5.

W4-5	W4-4	W4-7	W4-6	Comment
Off	Off	x	x	MMA master channel 0 to 3.
Off	On	Off	Off	MMA slave channel 0.
Off	On	Off	On	MMA slave channel 1.
Off	On	On	Off	MMA slave channel2.
Off	On	On	On	MMA slave channel 3.
On	x	x	x	Mubus interface.

Table 5: Interface configuration

- MMA master mode: in this mode the interface can control 4 MMA slaves connected on it. The on board FIFOs are disconnected in this mode.
- MMA slave mode: in this mode the interface is under the control of the master connected on it. The on board FIFOs are used to synchronise the data during the transfers. W4-6..W4-7 are used to set the channel number.
- Mubus mode: in this mode the interface operates as a simple 8 bit CPU interface.

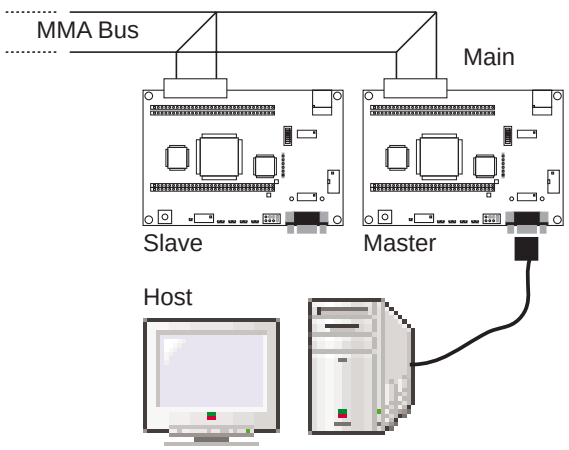

Figure 4: Multi-processor application

The local network KNet

This network interface allows the connection of a pool of Khepera processor turrets (see table 6 for the pinning connector).

J4: KNet connector			
AMP micro match 8 pin female connector			
Signal	Pin	I/O	Comment
GND	1	Power	Digital ground.
SCK	2	Digital O	Data clock..
MISO	3	Digital I	Master I Slave O.
MOSI	4	Digital O	Mastar O Slave I.
/SPCOM	5	Digital O	Network select..
PAI	6	Digital I	Acknowledge..
F7	7	Digital O	Strobe..
VCC	8	Power	+5V.

Table 6: KNet connector

This network (figure 5) is intended to export complicate pre or post processing algorithms close to sensors or actuators. The communication protocol implementation is K-Team property.

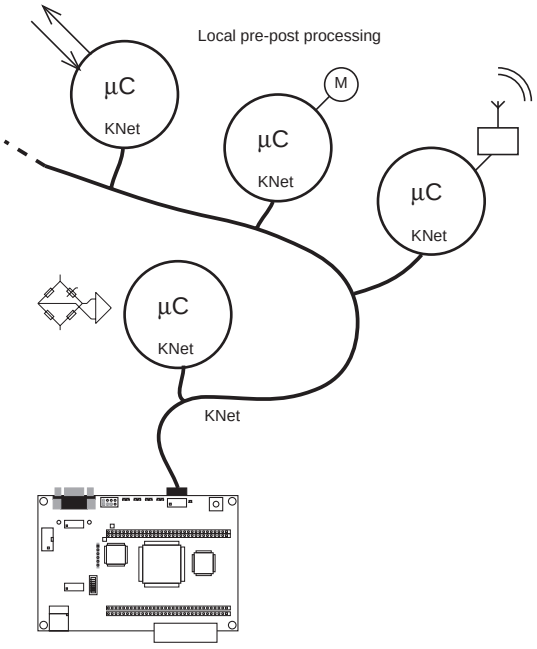

Figure 5: KNet topology

The CPU & Interface eXtension Busses

These buses allow the connection of additional boards (figure 6) designed for industrial interface extensions.

CXB is specially intended for interfaces using close interactions with the microcontroller (see table 7 for the pinning connector).

IXB is specially intended for interfaces using complicated temporal sequences or using analog or power devices (see table 8 for the pinning connector).

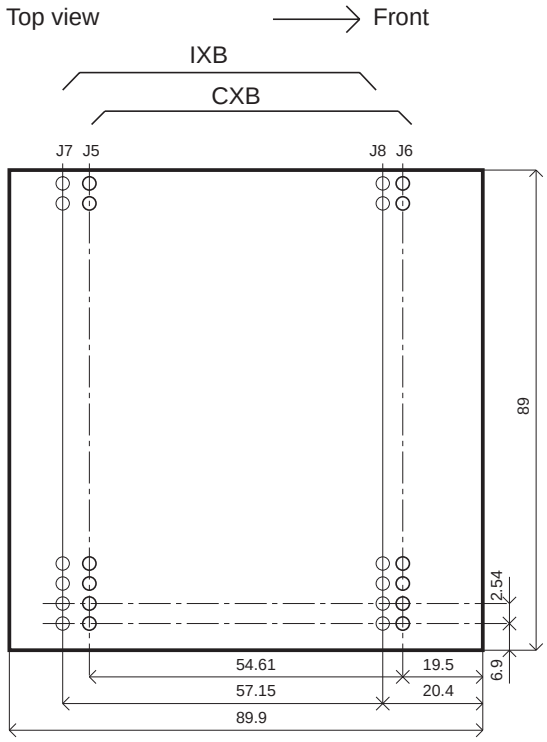

Figure 6: Mechanical draw of the CXB-IXB

J7: Interface eXtension Bus connector				J8: Interface eXtension Bus connector			
32 pin female connector				32 pin female connector			
Signal	Pin	I/O	Comment	Signal	Pin	I/O	Comment
GNA	1	Power	Analog ground.	CTM2C	1	Digital I	Ext.. clock.
PQA0	2	Analog I	Analog input A0.	CTD3	2	Digital I/O	Double action DASM3.
PQA1	3	Analog I	Analog input A1.	CTD4	3	Digital I/O	Double action DASM4.
PQA2	4	Analog I	Analog input A2.	CTD9	4	Digital I/O	Double action DASM9.
PQA3	5	Analog I	Analog input A3.	CTD10	5	Digital I/O	Double action DASM10.
PQA4	6	Analog I	Analog input A4.	CPWM5	6	Digital I/O	Double action PWMSM5.
PQA5	7	Analog I	Analog input A5.	CPWM6	7	Digital I/O	Double action PWMSM6.
PQA6	8	Analog I	Analog input A6.	CPWM7	8	Digital I/O	Double action PWMSM7.
PQA7	9	Analog I	Analog input A7.	CPWM8	9	Digital I/O	Double action PWMSM8.
PQB0	10	Analog I	Analog input B0.	GND	10	Power	Digital ground.
PQB1	11	Analog I	Analog input B1.	CH0	11	Digital I/O	TPU channel 0
PQB2	12	Analog I	Analog input B2.	CH1	12	Digital I/O	TPU channel 1
PQB3	13	Analog I	Analog input B3.	CH2	13	Digital I/O	TPU channel 2
PQB4	14	Analog I	Analog input B4.	CH3	14	Digital I/O	TPU channel 3
PQB5	15	Analog I	Analog input B5.	CH4	15	Digital I/O	TPU channel 4
PQB6	16	Analog I	Analog input B6.	CH5	16	Digital I/O	TPU channel 5
GNA	17	Power	Analog ground.	CH6	17	Digital I/O	TPU channel 6
GNA	18	Power	Analog ground.	CH7	18	Digital I/O	TPU channel 7
+VRef	19	Power	Ref. +4.096 V.	CH8	19	Digital I/O	TPU channel 8
+VRef	20	Power	Ref. +4.096 V.	CH9	20	Digital I/O	TPU channel 9
N.C.	21			CH10	21	Digital I/O	TPU channel 10
/Reset	22	Digital I/O	System reset.	CH11	22	Digital I/O	TPU channel 11
MISO	23	Digital I	Master I Slave O.	CH12	23	Digital I/O	TPU channel 12
MOSI	24	Digital O	Master O Slave I.	CH13	24	Digital I/O	TPU channel 13
SCK	25	Digital O	Data clock.	CH14	25	Digital I/O	TPU channel 14
/PCS1	26	Digital O	Select SPI1.	T2CLK	26	Digital I/O	TPU T2CLK
/PCS0	27	Digital O	Select SPI0.	GND	27	Power	Digital ground.
VCC	28	Power	+5 V.	GNP	28	Power	Power ground.
VCC	29	Power	+5 V.	GNP	29	Power	Power ground.
GND	30	Power	Digital ground.	GNP	30	Power	Power ground.
GND	31	Power	Digital ground.	+VInp	31	Power	+8.5 V to +20 V
GND	32	Power	Digital ground.	+VInp	32	Power	+8.5 V to +20 V

Table 7: IXB Interface eXtension Bus connector

J5: Interface eXtension Bus connector				J6: Interface eXtension Bus connector			
32 pin female connector				32 pin female connector			
Signal	Pin	I/O	Comment	Signal	Pin	I/O	Comment
GND	1	Power	Digital ground.	A0	1	Digital O	CPU address A0.
D0	2	Digital I/O	CPU data D0.	A1	2	Digital O	CPU address A1.
D1	3	Digital I/O	CPU data D1.	A2	3	Digital O	CPU address A2.
D2	4	Digital I/O	CPU data D2.	A3	4	Digital O	CPU address A3.
D3	5	Digital I/O	CPU data D3.	A4	5	Digital O	CPU address A4.
D4	6	Digital I/O	CPU data D4.	A5	6	Digital O	CPU address A5.
D5	7	Digital I/O	CPU data D5.	A6	7	Digital O	CPU address A6.
D6	8	Digital I/O	CPU data D6.	A7	8	Digital O	CPU address A7.
D7	9	Digital I/O	CPU data D7.	A8	9	Digital O	CPU address A8.
D8	10	Digital I/O	CPU data D8.	A9	10	Digital O	CPU address A9.
D9	11	Digital I/O	CPU data D9.	A10	11	Digital O	CPU address A10.
D10	12	Digital I/O	CPU data D10.	A11	12	Digital O	CPU address A11.
D11	13	Digital I/O	CPU data D11.	A12	13	Digital O	CPU address A12.
D12	14	Digital I/O	CPU data D12.	A13	14	Digital O	CPU address A13.
D13	15	Digital I/O	CPU data D13.	A14	15	Digital O	CPU address A14.
D14	16	Digital I/O	CPU data D14.	A15	16	Digital O	CPU address A15.
D15	17	Digital I/O	CPU data D15.	A16	17	Digital O	CPU address A16.
/CSExt4	18	Digital O	Extension select 4	A17	18	Digital O	CPU address A17.
/BErr	19	Digital I/O	Bus error.	A18	19	Digital O	CPU address A18.
/HALT	20	Digital I	System halt.	A19	20	Digital O	CPU address A19.
/IntEXT	21	Digital I	Interruption Req.	/AS	21	Digital O	Address strobe.
/CSExt5	22	Digital O	Extension select 5	/CSExt1	22	Digital O	Extension select 1.
/Reset	23	Digital I/O	System reset.	/CSExt2	23	Digital O	Extension select 2.
MISO	24	Digital I	Master I Slave O.	/CSExt3	24	Digital O	Extension select 3.
MOSI	25	Digital O	Master O Slave I.	SZ0	25	Digital O	Transfert size 0.
SCK	26	Digital O	Data clock.	SZ1	26	Digital O	Transfert size 1.
/PCS1	27	Digital O	Select SPI1.	/DSACK0	27	Digital I	Ack. transfer 0.
N.C.	28			/DSACK1	28	Digital I	Ack. transfer 1.
VCC	29	Power	+5 V.	R/W	29	Digital O	CPU R/W.
VCC	30	Power	+5 V.	GND	30	Power	Digital ground.
GND	31	Power	Digital ground.	CLKOut	31	Power	System clock.
GND	32	Power	Digital ground.	GND	32	Power	Digital ground.

Table 8: CXB CPU eXtension Bus connector

The Serial eXtension Bus (SXB)

This bus allows the connection of an additional board designed to increase the communication possibilities of the system (figure 7). An additional full RS232, RS422, SPI or CAN bus can be easily connected (see table 9 for the pinning connector).

J9: Serial eXtension Bus connector				J10: Serial eXtension Bus connector			
Erni 12 pin female connector				Erni 12 pin female connector			
Signal	Pin	I/O	Comment	Signal	Pin	I/O	Comment
VCC	A1	Power	+5 V..	VCC	A1	Power	+5 V.
/DCD	B1	Digital I	USART Carrier Detect.	Rx	B1	Digital I	USART Rx.
RI	A2	Digital I	USART Ring.	Tx	A2	Digital O	USART Tx.
Out1	B2	Digital O	USART general output 1.	GND	B2	Power	Digital ground.
Out2	A3	Digital O	USART general output 2.	GND	A3	Power	Digital ground.
RxCLK	B3	Digital I	Usart receiver clock.	GND	B3	Power	Digital ground.
BDCLK	A4	Digital O	USART Baud-rate clock.	/RTS	A4	Digital O	USART request To Send.
/Reset	B4	Digital I/O	System reset.	/CTS	B4	Digital I	USART Clear To Send.
MISO	A5	Digital I	Master I Slave O.	/DTR	A5	Digital O	USART Data Terminal Ready.
MOSI	B5	Digital O	Master O Slave I.	/DSR	B5	Digital I	USART Data Set Ready.
SCK	A6	Digital O	Data clock.	CANTx	A6	Digital O	CAN Tx.
/PCS3	B6	Digital O	Select SPI3.	CANRx	B6	Digital I	CAN Rx.

Table 9: SXB Serial eXtension Bus connector

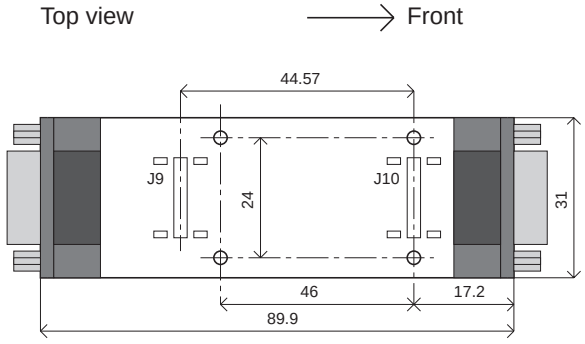

Figure 7: Mechanical draw of the SXB

The SXB module K376SXB-1 implements an additional full DTE-(DCE) RS232 channel and a CAN bus drivers.

The board arrangement

Figure 8 shows the board arrangement according with the schematics.

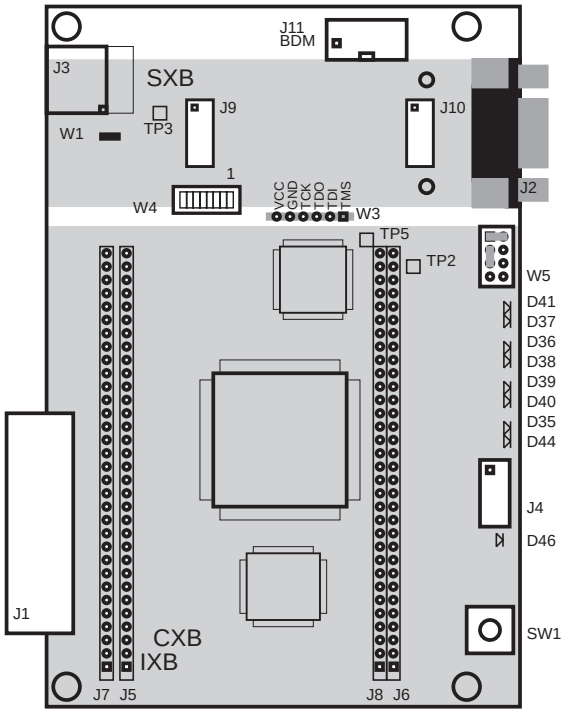

Figure 8: The board arrangement

Bootstrap modes

The multi-jumper W5 allows to configure different modes for the bootsrap (table 10).

W5	
A	**Normal configuration. Place the signal /AVEC on the pin 18 of the IXB interface connector. The bootstrap is performed by the code located inside the Flash.**
B	Place the signal /CSBoot on the pin 18 of the IXB interface connector. This allows to bootstrap the processor with a code located on a 16-bit device plugged on the IXB extension board. The on board Flash is controlled by the signal /CSExt4.
C	Place the signal /CSExt4 on the pin 18 of the IXB interface connector. The bootstrap is performed by the code located inside the Flash.
D	Place the signal /CSBoot on the pin 18 of the IXB interface connector. This allows to bootstrap the processor with a code located on a 8-bit device plugged on the IXB extension board. The on board Flash is controlled by the signal /CSExt4.

Table 10: Bootstrap modes

According with the settings of W4-0..W4-3 KOS can start in 8 different modes as described in table 11.

W4-3	W4-2	W4-1	Comment
Off	Off	Off	Reserved for future extension.
Off	Off	On	Launch the user program located inside the Flash. The communication channel is the COM set to 38400 bits/s.
Off	On	Off	Launch the SerCom environment. The communication channel is the MMA (see table 5).
Off	On	On	Reserved for future extension.
On	Off	Off	Reserved for future extension.
On	**Off**	**On**	**Launch the SerCom environment. The communication channel is the COM set to 38400 bits/s.**
On	On	Off	Reserved for future extension.
On	On	On	Erase the KOS. !!! Be sure to have the possibility to reload it from the K-Team Web server..

Table 11: Start-up modes

Start-up

Initialisation code used by the KOS to configure the main ressources of the K376SBC.

```
; Board mapping
; -------------

DebROM              = 16'000000               ; Flash (bootstrap code location)
 kLnROM             = (2**19)+(2**17)         ; lenght (640 K x 16)

DebFlash            = DebROM                  ; Flash
DebSystemFlash      = DebFlash+16'00000       ; 512 KBytes for the KOS
DebUserFlash        = DebFlash+16'80000       ; 512 KBytes for the user
 kLnFlash           = (2**18)+(2**17)         ; lenght (384 K x 16)

DebMeInt            = 16'100000               ; RAM
 kLnRam             = (2**20)                 ; lenght (512 K x 16)

DebUSART            = 16'200000               ; USART 16C450
DebExt1             = 16'300000               ; Extension 1
DebExt2             = 16'400000               ; Extension 2
DebExt3             = 16'500000               ; Extension 3
DebExt4             = 16'600000               ; Extension 4
DebIO               = 16'700000               ; misc I/O
 DebLEDs            = DebIO                   ; LEDs
 DebPAI             = DebIO+16'004            ; PAI
 DebMMA             = DebIO+16'040            ; MMA 0
 DebExtension       = DebIO+16'0C0            ; Mubus

; CS specifications
; -----------------

SPCS0  = ASYNC*(2**15)+BLU*(2**13)+Both*(2**11)+DS*(2**10)+W0*(2**6)+SUSP*(2**4)+LAll*(2**1)+AVOff*(2**0)
SPCS1  = ASYNC*(2**15)+BLU*(2**13)+Both*(2**11)+DS*(2**10)+W0*(2**6)+SUSP*(2**4)+LAll*(2**1)+AVOff*(2**0)
SPCS2  = ASYNC*(2**15)+BLU*(2**13)+Both*(2**11)+DS*(2**10)+W0*(2**6)+SUSP*(2**4)+LAll*(2**1)+AVOff*(2**0)
SPCS3  = ASYNC*(2**15)+BLU*(2**13)+Both*(2**11)+DS*(2**10)+W0*(2**6)+SUSP*(2**4)+LAll*(2**1)+AVOff*(2**0)
SPCS4  = ASYNC*(2**15)+BLU*(2**13)+Both*(2**11)+AS*(2**10)+W10*(2**6)+SUSP*(2**4)+LAll*(2**1)+AVOff*(2**0)
SPCS5  = SYNC*(2**15)+BLU*(2**13)+Read*(2**11)+AS*(2**10)+W0*(2**6)+CPUSP*(2**4)+L6*(2**1)+AVOn*(2**0)
SPCS6  = SYNC*(2**15)+BLU*(2**13)+Read*(2**11)+AS*(2**10)+W0*(2**6)+CPUSP*(2**4)+L4*(2**1)+AVOn*(2**0)
SPCS7  = SYNC*(2**15)+BLU*(2**13)+Read*(2**11)+AS*(2**10)+W0*(2**6)+CPUSP*(2**4)+L5*(2**1)+AVOn*(2**0)
SPCS8  = ASYNC*(2**15)+BLU*(2**13)+Both*(2**11)+AS*(2**10)+W1*(2**6)+SUSP*(2**4)+LAll*(2**1)+AVOff*(2**0)
SPCS9  = ASYNC*(2**15)+BUpper*(2**13)+Both*(2**11)+AS*(2**10)+W0*(2**6)+SUSP*(2**4)+LAll*(2**1)+AVOff*(2**0)
SPCS10 = ASYNC*(2**15)+BBLower*(2**13)+Both*(2**11)+AS*(2**10)+W0*(2**6)+SUSP*(2**4)+LAll*(2**1)+AVOff*(2**0)
SPCSBT = SIM_CSORBT,ASYNC*(2**15)+BLU*(2**13)+Both*(2**11)+AS*(2**10)+W0*(2**6)+SUSP*(2**4)+LAll*(2**1)+AVOff*(2**0)
```

```
; Configuration CPU table
; -----------------------

aTabIniSym:

; CS and I/O signal settings
       .32.16 SIM_CSPAR0,   CS8*(2**12)+CS8*(2**10)+CS16*(2**8)+CS16*(2**6)+CS16*(2**4)+CS16*(2**2)+CS16*(2**0)
       .32.16 SIM_CSPAR1,   CS16*(2**8)+CS16*(2**6)+CS8*(2**4)+CS16*(2**2)+A1Fu*(2**0)

; CS mapping
       .32.16 SIM_CSBAR0,   (DebExt1/16'100)+S1M
       .32.16 SIM_CSBAR1,   (DebExt2/16'100)+S1M
       .32.16 SIM_CSBAR2,   (DebExt3/16'100)+S1M
       .32.16 SIM_CSBAR3,   (DebExt4/16'100)+S1M
       .32.16 SIM_CSBAR4,   (DebUSART/16'100)+S2K
       .32.16 SIM_CSBAR5,   (2'1111111111111000)+S128K
       .32.16 SIM_CSBAR6,   (2'1111111111111000)+S128K
       .32.16 SIM_CSBAR7,   (2'1111111111111000)+S128K
       .32.16 SIM_CSBAR8,   (DebIO/16'100)+S2K
       .32.16 SIM_CSBAR9,   (DebMeInt/16'100)+S1M
       .32.16 SIM_CSBAR10,  (DebMeInt/16'100)+S1M

; CS specs.
       .32.16 SIM_CSOR0,    SPCS0
       .32.16 SIM_CSOR1,    SPCS1
       .32.16 SIM_CSOR2,    SPCS2
       .32.16 SIM_CSOR3,    SPCS3
       .32.16 SIM_CSOR4,    SPCS4
       .32.16 SIM_CSOR5,    SPCS5
       .32.16 SIM_CSOR6,    SPCS6
       .32.16 SIM_CSOR7,    SPCS7
       .32.16 SIM_CSOR8,    SPCS8
       .32.16 SIM_CSOR9,    SPCS9
       .32.16 SIM_CSOR10,   SPCS10
       .32.16 SIM_CSORBT,   SPCSBT
kNbTabIniSym  = (APC-aTabIniSym)/6

; Initialisation routine
; ----------------------

StPRG: move.16       #2'0100000111001110,SIM_MCR        ; MCR init. (bus monitor on)
       move.8        #(2**BME),SIM_SYPCR                ; Watch-dog off & BERR after 64 cycles
       move.16       #2'1001010000000000,SIM_SYNCR      ; System Clock to 22.018500/2 MHz
1$:    test.8        SIM_SYNCR+1:#SLOCK                 ; wait the locking of the PLL
       jump,bc       R8^1$                              ;
       move.16       #2'1101010000000000,SIM_SYNCR      ; System Clock to 22.018500 MHz

       move.16       #kNbTabIniSym-1,D0                 ; init. table size
       move.32       #R16^aTabIniSym,A0                 ; ptr on the init. table
m$:    move.32       {A0+},A1                           ; ptr on the register
       move.16       {A0+},{A1}                         ; data ---> register
       dj.16,nmo     D0,m$                              ; continue
       ...
```

Absolute maximum ratings

VDD:	+5 V
VRef:	+4.096 V
Main input voltage:	+8.5 V to +20 V DC
Digital inputs:	-0.3 V to VDD+0.5 V
Analog inputs:	-0.3 V to VRef+0.3 V
Operating temp:	0 ºC to +80 ºC

References

http://www.k-team.com

http://www.mcu.motsps.com/lit/manuals/376/mc68376.htm