TECHNICAL USER'S MANUAL FOR:

MICROSPACE®

PC/104*plus*
Peripheral boards

MSMFG104+
Frame-Grabber BT848

#070999-1

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Table of Contents

1 PREFACE

This manual is for integrators and programmers of systems based on the MicroSpace card family. It contains information on hardware requirements, interconnections, and details of how to program the system. The specifications given in this manual were correct at the time of printing; advances mean that some may have changed in the meantime. If errors are found, please notify DIGITAL-LOGIC AG at the address shown on the title page of this document, and we will correct them as soon as possible.

1.1 How to use this manual

This manual is written for the original equipment manufacturer (OEM) who plans to build computer systems based on the single board MicroSpace-PC. It provides instructions for installing and con-figuring the MSM104RS board, and describes the system and setup requirements.

1.2 Trademarks

Chips & Technologies	SuperState R
MicroSpace, MicroModule	DIGITAL-LOGIC AG
DOS Vx.y, Windows	Microsoft Inc.
PC-AT, PC-XT	IBM
NetWare	Novell Corporation
Ethernet	Xerox Corporation
DR-DOS, PALMDOS	Digital Research Inc. / Novell Inc.
ROM-DOS	Datalight Inc.

1.3 Disclaimer

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1.4 Who should use this product

- Electronic engineers with know-how in PC-technology.
- Without electronic know-how we expect you to have questions. This manual assumes, that you have a general knowledge of PC-electronics.
- Because of the complexity and the variability of PC-technology, we can't give any warranty that the product will work in any particular situation or combination. Our technical support will help you.
- Pay attention to the electrostatic discharges. Use a CMOS protected workplace.
- Power supply OFF when you are working on the board or connecting any cables or devices.

This is a high technology product.
You need know-how in electronics and PC-technology to install the system !

1.5 Recycling Information

Hardware:	**- Print:**	epoxy with glass fiber wires are of tin-plated copper
	- Components:	ceramics and alloys of gold, silver check your local electronic recycling
Software:	**- no problems:**	re-use the diskette after formatting

1.6 Technical Support

1. Contact your local DIGITAL-LOGIC Technical Support in your country.
2. Use Internet Support Request form on http://www.digitallogic.ch -> Support -> Support Request
3. Send a FAX or an E-mail to DIGITAL-LOGIC AG with a description of your problem.

DIGITAL-LOGIC AG
Technical Support dept.
Nordstrasse 11/F
CH-4542 Luterbach (SWITZERLAND)

Fax: ++41-32 681 53 31
E-Mail: support@digitallogic.ch

➔ Support requests will only be accepted with detailed informations about the product (BIOS-, Board-Version) !

1.7 Limited Warranty

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Before returning any product for repair, customers are required to contact the company.

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2 OVERVIEW

2.1 Ordering Information

MSMFG104+	Frame Grabber

2.2 General Information

BUS:

Standard:	PC/104+
Size:	32Bit PCI

Power Supply:

Power:	Working: 5Volt / 1W

Physical Characteristics:

Dimensions:	Length: 90mm
	Width: 96mm
	Height: 15mm

Operating Environment:

Relative humidity:	5 - 90% non condensing		
Vibration:	5 to 2000 Hz		
Shock:	10g		
Temperature:	Operating:	Standard version:	-25°C to +70°C
		Industry version:	-25°C to +85°C (ask DIGITAL-LOGIC AG)
	Storage:	-55°C to 85°C	

2.3 Frame Grabber

Framegrabber Interface:

Controller:	BT 848A	Brooktree
Enhanced BIOS:	none	
Memory:	none	
Interface:	4 x Coax	
Driver:	ask DIGITAL-LOGIC AG for drivers	

Any information is subject to change without notice.

2.4 Driver Support

Product:	Driver for:	Internet Link to the supplied drivers
IDE	WIN CE V2.11	http://developer.intel.com/platforms/applied/software/
CT69000 CT65554 CT65548	Win CE V2.11 QNX / Neutrino WIN95/WIN98/NT4 WIN CE V2.11	http://developer.intel.com/platforms/applied/software/ http://www.qnx.com/products/hardware/photon_video.txt http://developer.intel.com/support/graphics/mobile/software.htm http://www.annasoft.com/cetop.htm
Intel 82259	Win CE V2.11 VxWorks 5.3.1. QNX / Neutrino	http://developer.intel.com/platforms/applied/software/ http://developer.intel.com/platforms/applied/software/ http://www.qnx.com/products/hardware/network_support.html
SMC 91C94/96	QNX / Neutrino WIN95/98/NT4/WIN-CE WIN-CE	http://www.qnx.com/products/hardware/network_support.html http://www.smsc.com/ftpdocs/chips.html http://www.annasoft.com/cetop.htm
SCSI AIC7860/70	QNX / Neutrino WIN95/WIN98/NT4/DOS	http://www.qnx.com/products/hardware/scsi_support.html http://www.adaptec.com/support/overview/aha2940au.html
SCSI NCR 53810	QNX / Neutrino DOS/WIN95/WIN98/NT4 Novell/SCO UnixWare/Solaris7	http://www.qnx.com/products/hardware/scsi_support.html http://www.lsilogic.com/products/pci_sw http://www.lsilogic.com/products/pci_sw
PCMCIA	QNX / Neutrino WIN95/98 and NT4 WIN98 / NT4	http://www.qnx.com/products/hardware/pcmcia_support.html http://www.systemsoft.com/products/pccard/index.htm http://www.phoenix.com
Sound ESS 1869	QNX / Neutrino WIN95/WIN98/NT4/DOS	http://www.qnx.com/products/hardware/audio_support.txt http://www.esstech.com/

Product:	Driver for:	Internet Link to the supplied drivers
DOC2000 M-Systems	DOS / WIN95 / NT4 /CE 2.11, LINUX 2.x, QNX 4.23/4.24	http://www.m-sys.com/ http://www.m-sys.com/
Datalight FFS	DOS / QNX / WIN-CE	http://www.datalight.com/flash.htm
AMI BIOS	BIOS Tools	http://www.ami.com/
Phoenix BIOS	BIOS Tools	http://www.phoenix.com
ELO-Touch	DOS, WIN95, NT4	http://www.elotouch.com/library.html
ZORAN	NT4, WIN95	http://www.zoran.com/ftp/download/refdesigns/h33
Philips SAA7111	diverse	http://www-us2.semiconductors.philips.com/pip/SAA7111AH
GENESIS	Code	no online drivers available
Linux		www.linux.com

3 PC/104 BUS SIGNALS

AEN, output
Address Enable is used to degate the microprocessor and other devices from the I/O channel to allow DMA transfers to take place. **low = CPU Cycle , high = DMA Cycle**

BALE, output
Address Latch Enable is provided by the bus controller and is used on the system board to latch valid addresses and memory decodes from the microprocessor. This signal is used so that devices on the bus can latch LA17..23. The SA0..19 address lines latched internally according to this signal. BALE is forced high during DMA cycles.

/DACK[0..3, 5..7], output
DMA Acknowledge 0 to 3 and 5 to 7 are used to acknowledge DMA requests (DRQO through DRQ7). They are **active low**. This signal indicates that the DMA operation can begin.

DRQ[0..3, 5..7], input
DMA Requests 0 through 3 and 5 through 7 are asynchronous channel requests used by peripheral devices and the I/O channel microprocessors to gain DMA service (or control of the system). A request is generated by bringing a DRQ line to an active level. A DRQ line must be held high until the corresponding DMA Request Acknowledge (DACK/) line goes active. DRQO through DRQ3 will perform 8-Bit DMA transfers; DRQ5-7 are used for 16 accesses.

/IOCHCK, input
IOCHCK/ provides the system board with parity (error) information about memory or devices on the I/O channel. **low = parity error, high = normal operation**

IOCHRDY, input
I/O Channel Ready is pulled low (not ready) by a memory or I/O device to lengthen I/O or memory cycles. Any slow device using this line should drive it low immediately upon detecting its valid address and a Read or Write command. Machine cycles are extended by an integral number of one clock cycle (67 nanoseconds). This signal should be held low for no more than 2.5 microseconds. **low = wait, high = normal operation**

/IOCS16, input
I/O 16 Bit Chip Select signals the system board that the present data transfer is a 16-Bit, 1 wait-state, I/0 cycle. It is derived from an address decode. /IOCS16 is **active low** and should be driven with an open collector (300 ohm pull-up) or tri-state driver capable of sinking 20mA. The signal is driven based only on SA15-SAO (not /IOR or /IOW) when AEN is not asserted. In the 8 Bit I/O transfer, the default transfers a 4 wait-state cycle.

/IOR, input/output
I/O Read instructs an I/O device to drive its data onto the data bus. It may be driven by the system microprocessor or DMA controller, or by a microprocessor or DMA controller resident on the I/O channel. This signal is **active low**.

/IOW, input/output
I/O Write instructs an I/O device to read the data on the data bus. It may be driven by any microprocessor or DMA controller in the system. This signal is **active low**.

IRQ[3 - 7, 9 - 12, 14, 15], input
These signals are used to tell the microprocessor that an I/O device needs attention. An interrupt request is generated when an IRQ line is **raised from low to high**. The line must be held high until the microprocessor acknowledges the interrupt request.

/Master, input
This signal is used with a DRQ line to gain control of the system. A processor or DMA controller on the I/0 channel may issue a DRQ to a DMA channel in cascade mode and receive a /DACK.

/MEMCS16, input
MEMCS16 Chip Select signals the system board if the present data transfer is a 1 wait-state, 16-Bit, memory cycle. It must be derived from the decode of LA17 through LA23. /MEMCS16 should be driven with an open collector (300 ohm pull-up) or tri-state driver capable of sinking 2OmA.

/MEMR input/output
These signals instruct the memory devices to drive data onto the data bus. /MEMR is active on all memory read cycles. /MEMR may be driven by any microprocessor or DMA controller in the system. When a microprocessor on the I/0 channel wishes to drive /MEMR, it must have the address lines valid on the bus for one system clock period before driving /MEMR active. These signals are **active low**.

/MEMW, input/output
These signals instruct the memory devices to store the data present on the data bus. /MEMW is active in all memory read cycles. /MEMW may be driven by any microprocessor or DMA controller in the system. When a microprocessor on the I/O channel wishes to drive /MEMW, it must have the address lines valid on the bus for one system clock period before driving /MEMW active. Both signals are **active low.**

OSC, output
Oscillator (OSC) is a high-speed clock with a 70 nanosecond period (14.31818 MHz). This signal is not synchronous with the system clock. It has a 50% duty cycle. OSC starts 100µs after reset is inactive.

RESETDRV, output
Reset Drive is used to reset or initiate system logic at power-up time or during a low line-voltage outage. This signal is active high. When the signal is active all adapters should turn off or tri-state all drivers connected to the I/O channel. This signal is driven by the permanent Master.

/REFRESH, input/output
These signals are used to indicate a refresh cycle and can be driven by a microprocessor on the I/0 channel. These signals are **active low**.

SAO-SA19, LA17 - LA23 input/output
Address bits 0 through 19 are used to address memory and I/0 devices within the system. These 20 address lines, allow access of up to 1MBytes of memory. SAO through SA19 are gated on the system bus when BALE is high and are latched on the falling edge of BALE. LA17 to LA23 are not latched and addresses the full 16 MBytes range. These signals are generated by the microprocessors or DMA controllers. They may also be driven by other microprocessor or DMA controllers that reside on the I/0 channel. The SA17-SA23 are always LA17-LA23 address timings for use with the MSCS16 signal. This is advanced AT96 design. The timing is selectable with jumpers LAxx or Saxx.

/SBHE, input/output
Bus High Enable (system) indicates a transfer of data on the upper byte of the data bus, XD8 through XD15. Sixteen-Bit devices use /SBHE to condition data-bus buffers tied to XD8 through XD15.

SD[O..15], input/output
These signals provide bus bits 0 through 15 for the microprocessor, memory, and I/0 devices. DO is the least-significant Bit and D15 is the most significant Bit. All 8-Bit devices on the I/O channel should use DO through D7 for communications to the microprocessor. The 16-Bit devices will use DO through D15. To support 8-Bit device, the data on D8 through D15 will be gated to DO through D7 during 8-Bit transfers to these devices; 16-Bit microprocessor transfers to 8-Bit devices will be converted to two 8-Bit transfers.

/SMEMR input/output
These signals instruct the memory devices to drive data onto the data bus for the first MByte. /SMEMR is active on all memory read cycles. /SMEMR may be driven by any microprocessor or DMA controller in the system. When a microprocessor on the I/0 channel wishes to drive /SMEMR, it must have the address lines valid on the bus for one system clock period before driving /SMEMR active. The signal is **active low**.

/SMEMW, input/output
These signals instruct the memory devices to store the data present on the data bus for the first MByte. /SMEMW is active in all memory read cycles. /SMEMW may be driven by any microprocessor or DMA controller in the system. When a microprocessor on the I/O channel wishes to drive /SMEMW, it must have the address lines valid on the bus for one system clock period before driving /SMEMW active. Both signals are **active low.**

SYSCLK, output
This is a 8 MHz system clock. It is a synchronous microprocessor cycle clock with a cycle time of 167 nanoseconds. The clock has a 66% duty cycle. This signal should only be used for synchronization.

TC output
Terminal Count provides a pulse when the terminal count for any DMA channel is reached. The TC completes a DMA-Transfer. This signal is expected by the onboard floppy disk controller. Do not use this signal, because it is internally connected to the floppy controller.

/OWS, input
The Zero Wait State (/OWS) signal tells the microprocessor that it can complete the present bus cycle without inserting any additional wait cycles. In order to run a memory cycle to a 16-Bit device without wait cycles, /OWS is derived from an address decode gated with a Read or Write command. In order to run a memory cycle to an 8-Bit device with a minimum of one-wait states, /OWS should be driven active one system clock after the Read or Write command is active, gated with the address decode for the device. Memory Read and Write commands to an 8-Bit device are active on the falling edge of the system clock. /OWS is **active low** and should be driven with an open collector or tri-state driver capable of sinking 2OmA.

12V +/- 5%
used only for the flatpanel supply and BIAS generation.

GROUND = 0V
used for the entire system.

VCC, +5V +/- 0.25V
separate for logic and harddisk/floppy supply.

3.1 Expansion Bus

Only the PCI Bus is used.

4 DETAILED SYSTEM DESCRIPTION

The description of the BT848 use the datasheet on the DIGITAL-LOGIC developer application CD.

5 CONNECTORS ON THE BOARD

Connector:	Function:	Remarks:
J11	Videoinput 2	Videosource
J12	VideoInput 1	Videosource
J13	VideoInput 0	Videosource
J14	CVBS Input	CVBS Source
J15	VideoInput 3	VideoSource
J16	only for internal test	do not use this connector

6 JUMPER LOCATIONS ON THE BOARD

6.1 The Jumpers on this MICROSPACE product

J6 PCI-Bus Clocksource	open	close
1-2	none	PCICLK 0
3-4	none	PCICLK 1
5-6	none	PCICLK 2
7-8	none	PCICLK 3

Only one of this selection may be closed. Use a signal, where is from no other board used.

J7 PCI-GRANT Source	open	close
1-2	none	GNT 0
3-4	none	GNT 1
5-6	none	GNT 2
7-8	none	GNT 3

Only one of this selection may be closed. Use a signal, where is from no other board used. J7 and J10 must be on the same number!

J8 PCI-IDSEL Source	open	close
1-2	none	ID 0
3-4	none	ID 1
5-6	none	ID 2
7-8	none	ID 3

Only one of this selection may be closed. Use a signal, where is from no other board used.

J9 PCI-IRQ Source	open	close
1-2	none	IRQ A
3-4	none	IRQ B
5-6	none	IRQ C
7-8	none	IRQ D

Only one of this selection may be closed. Use a signal, where is from no other board used.

J10 PCI-REQUEST Source	open	close
1-2	none	REQ 0
3-4	none	REQ 1
5-6	none	REQ 2
7-8	none	REQ 3

Only one of this selection may be closed. Use a signal, where is from no other board used. J10 and J7 must be on the same number.

*** = Default**

6.2 The part schematics of the MSMFG104